CLAIMS

Having thus described the invention, what is claimed is:

1. A method of fabricating at least a pair of local interconnects with one interconnect on each side of a gate of a field effect transistor (FET) in an integrated circuit on a semiconductor substrate comprising the steps of:

forming on a semiconductor substrate a thick insulating layer;

forming at least a pair of spaced apart openings in the insulating layer adjacent the semiconductor substrate;

forming a source in one of the openings and a drain in the other of the openings;

filling each of the openings with a conductive material to form local interconnects to the source and drain;

removing a portion of the insulating layer to form a gate opening between the local interconnects;

forming a gate dielectric on the semiconductor substrate in the gate opening; and

forming a gate on the gate dielectric oxide in the gate opening between the local interconnects.

2. The method of Claim 1, wherein the space between the pair of openings is one minimum photolithographic feature and the local interconnects are each one minimum photolithographic feature.

3. The method of Claim 1, wherein insulating spacers are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate.

4. The method of Claim 1, wherein the source and drain are formed by implanting impurities in the pair of openings in the insulating layer.

5. The method of Claim 1, wherein the portion of insulating layer removed to form the gate opening is removed by using a masking material with an opening in the masking material positioned between the pair of local interconnects.

6. The method of Claim 5, wherein the opening in the masking material extends over but not beyond each of the pair of local interconnects.

7. The method of Claim 6, wherein the spaced apart openings are positioned over an active region in the semiconductor substrate, the active region being surrounded by an isolation region, the openings extending to or beyond the active region.

8. The method of Claim 1, wherein a conductive layer is formed on the walls of the spaced apart openings to line the openings and a remainder of the local interconnect openings are filled with another conductive material.

9. The method of Claim 8, wherein the conductive layer is polysilicon and the other conductive material is tungsten.

10. The method of Claim 9, wherein the polysilicon is the origin for the impurities for the source and drain.

11. The method of Claim 1, wherein a barrier layer is formed on walls of the local interconnect openings to line the opening and a remainder of the local interconnect opening is filled with a conductive material.

12. The method of Claim 11, wherein the barrier layer includes titanium nitride.

13. The method of Claim 1, wherein an insulating etch stop layer is formed on semiconductor substrate before forming the thick insulating layer.

14. The method of Claim 13, wherein the etch selectivity of the etch stop layer is different from the etch selectivity of the insulating layer.

15. The method of Claim 14, wherein the etch stop layer is a nitride of silicon.

16. The method of Claim 1, wherein the gate is selected from the group of polysilicon, refractory metal and metal.

17. In a method of fabricating, in an integrated circuit on a semiconductor substrate, a field effect transistor (FET) having a source, drain and gate and with one interconnect on each side of a gate of the FET comprising the steps of:

forming on a semiconductor substrate a thick insulating layer;

forming a pair of spaced apart openings in the insulating layer adjacent the semiconductor substrate, each opening being the size of a minimum lithographic feature;

forming a source in one of the openings and a drain in the other of the openings;

filling each of the openings with a conductive material to form local interconnects to the source and drain;

removing a portion of the insulating layer to form a gate opening of a minimum lithographic feature between the local interconnects; and

forming a gate in the gate opening between the local interconnects, whereby the size of the FET transistor is three minimum lithographic features.

18. The method of Claim 17, wherein openings in the insulating material are positioned over an active region in the semiconductor substrate, the active region being surrounded by an isolation region, and the openings extending to or beyond the active region.

19. An integrated circuit including at least one transistor, the integrated circuit comprising:

a pair of local interconnects spaced from each other by a minimum lithographic feature and each being a minimum lithographic feature; and

a gate of the transistor disposed in the space between the local interconnects and separated from each of the local interconnects by an insulating liner, whereby the width of the transistor is not greater than three lithographic features.

20. The integrated circuit of Claim 19, wherein insulating spacers are each disposed on a interconnect wall adjacent the gate to separate each of the local interconnects from the gate.

21. An integrated circuit including at least one transistor, the integrated circuit comprising:

a pair of local interconnects spaced from each other; and

a gate of the transistor disposed in the space between the local interconnects and separated from each of the local interconnects by an insulating liner.

22. The integrated circuit of Claim 21, wherein the pair of local interconnects are spaced from each other by a minimum lithographic feature.

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